datelcare

Datelcare bv,
P.O. box 2,
3700 AA Zeist,
The Netherlands

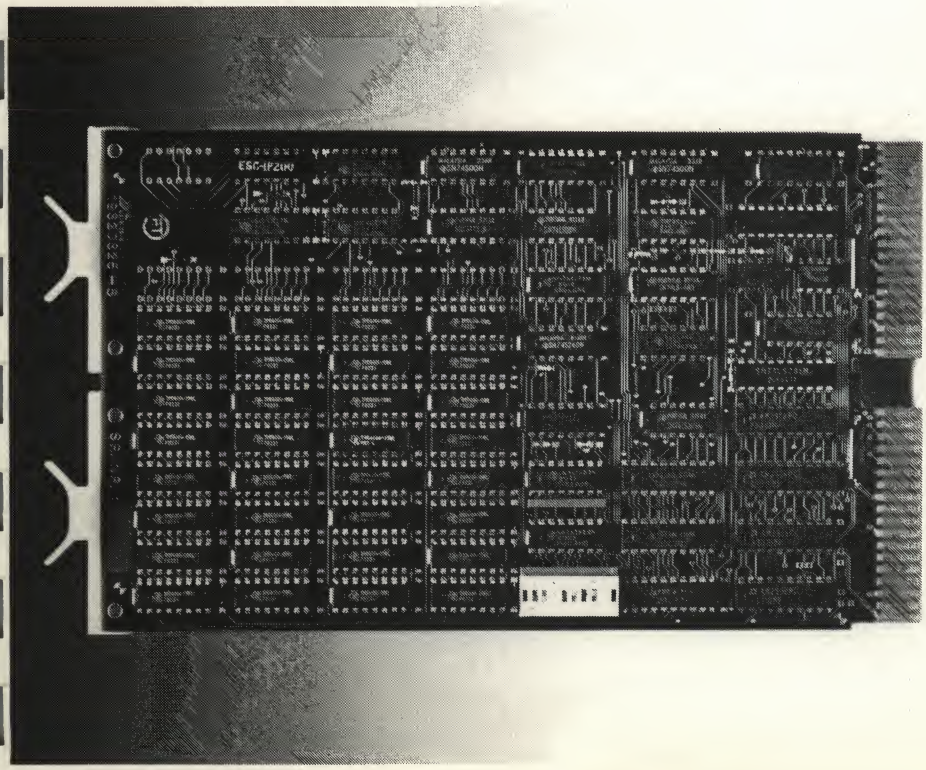
256 KILO BYTE ADD-IN MOS MEMORIES FOR Q-BUS BASED COMPUTER SYSTEMS.

General

Datelcare combines its long experience with the reliability of state of the art 64 K dynamic RAMs to offer memories that will improve the performance of all systems based on 11/23 or 11/23-plus cpu's.

Low-cost and superior quality are features that are standard on all DTC products. The DTC-256 is compatible with all 16, 18 and 22 bit addressing schemes used on Q-bus systems. A one bit per byte parity is included in all modules.

Depopulated versions can be provided for use in 11/02 and 11/21 (Falcon) based systems.



DTC-256 memories allow 4 MB addressing when used in 11/23 or 11/23-plus based computer systems, so minimizing swapping and further improving system-throughput.

This dual-width module needs a single + 5 volt supply only. Power consumption is typically less then 7.5 watts. This means less heat dissipation and a lower demand on the system's power supply.

Features

* 256 KByte module
* Standard dual-width board
* 4 MB addressing capability
* Includes parity bits
* Depopulated versions available
* Supports battery backup
* Fast 190 ns access time
* Compatible with all DEC hardware, diagnostics and software
* Needs only a single +5 volt supply

Installation

DTC-256 memory modules can be installed in any Q-bus backplane. The 22 bit addressing scheme however requires a backplane that has all 22 address lines implemented.

All DTC-20/23xx and DEC 11/23-plus based systems are provided with this feature. If in doubt, consult your supplier.

Parity

A 2 bit per word parity system is included in all DTC-256 modules. All 11/23 and 11/23-plus based systems sense parity for each memory-read cycle.

This method is fully compatible with DEC's MSV11-E memory modules.

Part numbers

DTC-256 - 256 KB	includes parity
DTC-128 - 128 KB	includes parity
DTC-064 - 64 KB	without parity, for use in 11/02 and 11/21 systems
DTC-032 - 32 KB	without parity, for use in 11/02 and 11/21 systems

Specifications:

Timing:

Function	Access time	Cycle time
DATI	190 ns	490 ns
DATO (B)	90 ns	390 ns
DATIO (B)	700 ns	1000 ns

During memory refresh a delay of up to 500 ns can occur.

Power supply: + 5 Volt 1,5 A maximum

Quality assurance

Datelcare guarantees that all its products are built to the highest commercial standards. All modules are fully tested and temperature cycled prior to shipment.

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TECNICAL MANUAL

DTC XXX MEMORY BOARDS

(board rev B and C)

REV C1

DATELCARE
ZEIST
THE NETHERLANDS

Contents

CHAPTER 1 GENERAL DESCRIPTION

1.1 Introduction

This manual applies to the following DATELCARE Q-bus memory boards, (hardware rev B).

DTC 256 P	DTC 64 P
DTC 256	DTC 64
DTC 128 P	DTC 32 P
DTC 128	DTC 32

Chapter 1 gives general information and specifications.

Chapter 2 contains all necessary information for installing the memory board.

Chapter 3 informs about the necessary maintenance.

Chapter 4 contains all electrical and mechanical drawings.

Chapter 5 deals with "engeneering change orders" (ECO's).

1.2.Purpose

The DTC-256 is a 128 KW (16 bit word) dynamic NMOS read/write memory module. It can be used in LSI-11/23 (PDP11/23) computer systems. The memory features 22 bit addressing for a maximum capacity of 2 MW (4 megabyte). Depopulated versions are available for use in LSI-11 (PDP 11/03) systems where addressability is limited to 28 KW (56 KB).
Memory refresh is performed automatically by internal logic and requires no cpu-interference.

1.3 Specifications

1.3.1 Physical dimensions

PCB	thickness	: 1.6 mm	
	width	: 133 mm	
	length	: 229 mm	(including plastic handles)
	max comp. height	: 10 mm	
	total thickness	: 12.5 mm	

1.3.2 Operating environment

Temperature : ambient air temperature range of 0 to +55 degrees C
Thermal shock : 30 degrees C per hour
Humidity : 0 to 95% relative humidity (non condensing)
Cooling : Suggested air flow of 25 cfm

1.3.3 Shipping environment

Temperature : the DTC memory can withstand a temperature range of -40 to +85 degrees C during shipping and storage.
Thermal shock : 10 degrees C per minute.
Mechanical shock : The DTC memory module housed in its shipping-container can withstand a mechanical shock resulting of a drop conforming to test in accordance with MIL-STD-810B, method 516, procedure V without any damage or degradation.

1.3.4 Power requirements

The DTC memory modules require a single 5 volt supply only. The DTC-256 memory card (256 KB) draws 1.5 A from a 5 volt (+/- 5%) supply. (Unit takes 680 mA from battery backup).

1.3.5 Timing

Function	Access time	Cycle time
DATI	190 ns	490 ns
DATO (B)	90 ns	390 ns
DATIO (B)	700 ns	1000 ns

During memory refresh a delay of up to 500 ns can be added to the above times.

1.3.6 Reliability

The DTC memory modules are designed to meet the best commercial standards of workmanship. Extensive testing is conducted to ensure a reliable service over the products' lifetime.
The memory chips used in the DTC 256 cards have a failure rate due to alpha partical radiation of 350 FIT (bit failures per 1,000,000,000 hours). This means that under normal circumstances an average of one soft error every 150 years (!) will occur.

1.4 Options

1.4.1 Capacity

The DTC memory cards are available with different capacity. The capacity is indicated by the number of the card name. The suffix P indicates that the memory card is equipped with parity memory chips.

DTC 256 P	128 K Words x 18 bits
DTC 256	128 K Words x 16 bits
DTC 128 P	64 K Words x 18 bits
DTC 128	46 K Words x 16 bits
DTC 64 P	32 K Words x 18 bits
DTC 64	32 K Words x 16 bits
DTC 32 P	16 K Words x 18 bits
DTC 32	16 K Words x 16 bits

1.4.2 Parity

DTC memory boards can be delivered with or without parity logic, depend on type of memory board. The parity option is compatible with the DEC MSV11-E memory modules.

CHAPTER 2 INSTALLATION

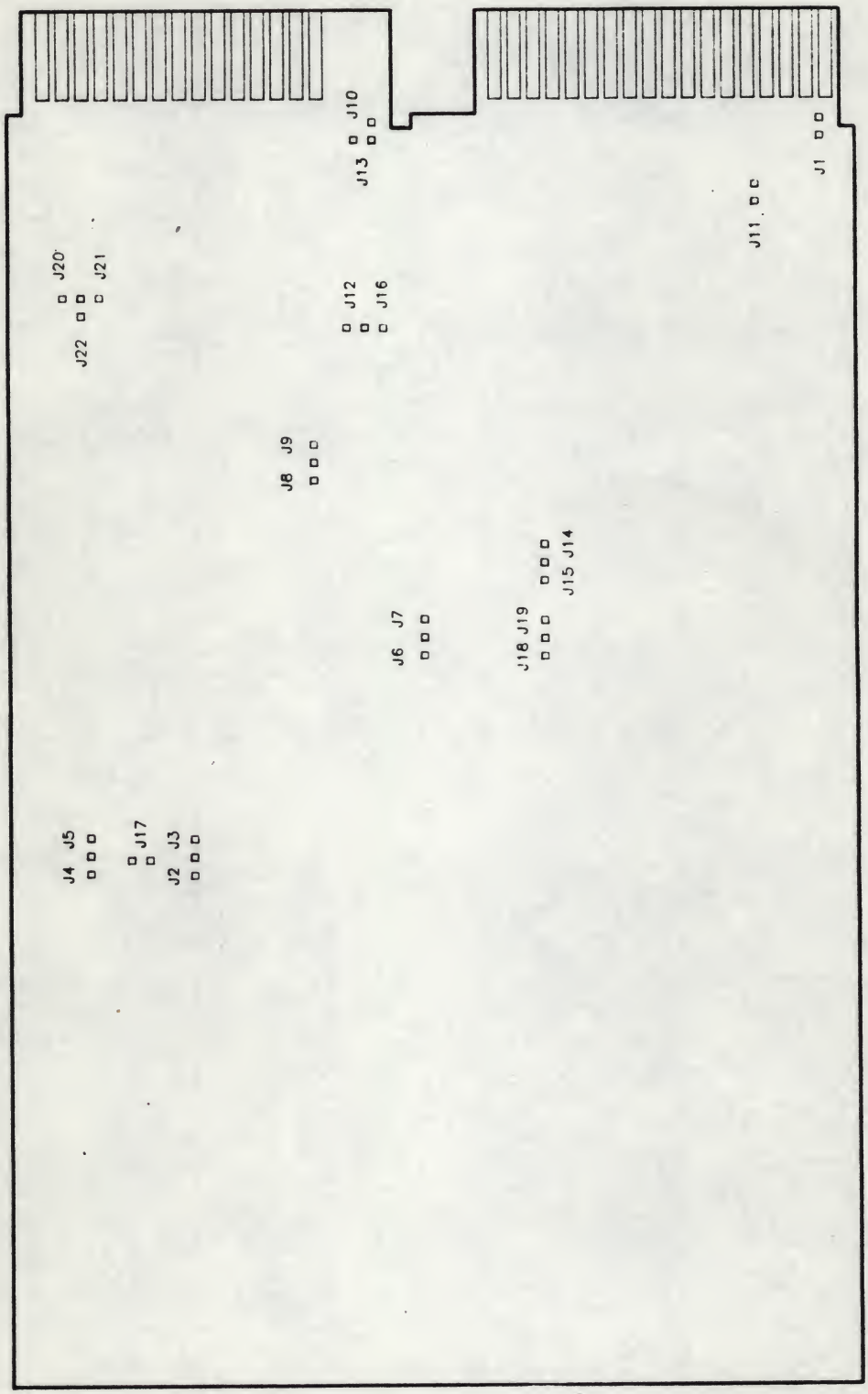


Figure 1. Jumper positions

The section contains information on procedures to install DTC memory modules in Q-bus computer systems.

Installation should be performed by qualified personnel only. Incorrect installation cannot only damage the memory board, but also all other system components.

After carefully unpacking the memory board, it should be inspected for any physical damage. IF any damage is found or expected, contact your distributor and do not install the board.

2.1 Address selection

When installing the memory board, the starting address, the bank size have to be determined. In a 18 bit-address space systems (LSI 11, LSI 11/02 and LSI 11/23) the 22 bits addressing feature of the memory boards have to be disabled, (jumper J12 and J16). The DTC memory board will automatically recognise when the I/O page is addressed.

2.1.1 Bank Selection

Switches S6 though S9 determine the bank in which the DTC memory will recognise the standard 18 address bits. In table 1 the switch settings are given.

TABLE 1

Bank (in words)	Switch setting S6	S7	S8	S9	
0 K - 128 K	I	I	I	I	no 22 bit addressing
0 K - 128 K	I	I	I	I	22 bit addressing
128 K - 256 K	0	I	I	I	
256 K - 384 K	I	0	I	I	
384 K - 512 K	0	0	I	I	
512 K - 640 K	I	I	0	I	
640 K - 768 K	0	I	0	I	
768 K - 896 K	I	0	0	I	
896 K - 1024 K	0	0	0	I	
1024 K - 1152 K	I	I	I	0	
1152 K - 1280 K	0	I	I	0	
1280 K - 1408 K	I	0	I	0	
1408 K - 1536 K	0	0	I	0	
1536 K - 1664 K	I	I	0	0	
1664 K - 1792 K	0	I	0	0	
1792 K - 1920 K	I	0	0	0	
1920 K - 2048 K	0	0	0	0	

I = switch closed (on)
0 = switch open (off)

2.1.2 Start address selection

Within the selected bank, the start address of the memory can be selected in 4 K Word increments with switches S1 - S5. When the combination of memory size and starting address is such that the bank upper boundary is crossed, that part of the memory is inaccessable.
The switch settings are given in table 2.

TABLE 2

Offset (in words)	Switch settings S1	S2	S3	S4	S5
0 K	0	0	0	0	0
4 K	I	0	0	0	0
8 K	0	I	0	0	0
12 K	I	I	0	0	0
16 K	0	0	I	0	0
20 K	I	0	I	0	0
24 K	0	I	I	0	0
28 K	I	I	I	0	0
32 K	0	0	0	I	0
36 K	I	0	0	I	0
40 K	0	I	0	I	0
44 K	I	I	0	I	0
48 K	0	0	I	I	0
52 K	I	0	I	I	0
56 K	0	I	I	I	0
60 K	I	I	I	I	0
64 K	0	0	0	0	I
68 K	I	0	0	0	I
72 K	0	I	0	0	I
76 K	I	I	0	0	I
80 K	0	0	I	0	I
84 K	I	0	I	0	I
88 K	0	I	I	0	I
92 K	I	I	I	0	I
96 K	0	0	0	I	I
100 K	I	0	0	I	I
104 K	0	I	0	I	I
108 K	I	I	0	I	I
112 K	0	0	I	I	I
116 K	I	0	I	I	I
120 K	0	I	I	I	I
124 K	I	I	I	I	I

0 = switch open (off)
I = switch closed (on)

2.1.3 Extended addressing selection

All DTC memory modules respond to 22 bit addressing for a total of up to 4 megabyte per system. This feature is compatible with all 11/23-plus systems as well as almost all other 11/23 systems already installed in the field.

22 bits addressing is selected according to Table 3.

TABLE 3

18/22 bits addressing

	22 bits	18 bits
J12	I	0
J16	0	I

2.2 Configuration selection

2.2.1 Memory size

The memory size can be reduced from 256 Kb to 32 Kb by means of jumpers J1, J6, J7, J11, J14, J15, J18, J19. (For rev C boards also jumpers J20, J21 and J22). The DTC 032 cards are equipped with 2118 DRAM's and a special configuration of the jumpers is necessary. Table 4 gives the configuration.

Note: the DTC memory boards are NOT upgradable by the user for a larger size than originally produced. Trying to install extra memory chips and jumper accordingly will damage the board.

TABLE 4

Jumper	Memory size (KB) (SEE NOTE AT 2.1.1) 32 2118 only	32	64	128	256
J 1	0	I	I	0	0
J 6	I	I	I	0	0
J 7	0	0	0	I	I
J11	I	0	0	0	0
J14	I	I	I	I	0
J15	0	0	0	0	I
J18	I	I	0	0	0
J19	0	0	I	I	I
J20*	0	0	0	0	0
J21*	I	I	I	I	0
J22*	0	0	0	0	I

I = jumper installed
0 = jumper removed

* = Board rev C only

2.3 Option selections

2.3.1 Parity

The DTC memory series are equipped with parity logic. This logic can be disabled or enabled with jumpers J2, J3, J4, J5, J17 as given in table 5.

TABLE 5

	parity	no parity
J 2	I	I
J 3	0	0
J 4	I	0
J 5	0	0
J17	0	I

I = installed
0 = removed

2.3.2 Battery back-up

*** NOTE ***
Board rev B and C has to be modified.
(ECO # 004)

When your system is equipped with a battery back-up unit, the DTC memory can be put on that unit by installing jumper J10 and removing jumper J13.

TABLE 6

	battery backing	no battery back-up
J10	I	0
J13	0	I

2.3.3 Refresh generator

Provisions have been made to control the refresh of the memory externally. This can be useful when the memory is used in special real-time DMA environment.
Normally the refresh cycle is generated on board and transparant to the user. However, an extra 500 ns delay in the memory access time will be introduced periodically.
Internal or external refresh can be selected with jumpers J8 and J9 according to table 7.

TABLE 7

Refresh jumper	internal	external
J8	0	I
J9	I	0

2.4 Initial Inspection

After carefully unpacking the memory board, it should be inspected for any physical damage. If any damage is found or expected, contact your distributor and do not install the board.
Installing a damaged board can possibly damage all other boards in your system.

2.5 Required tools and materials

No special tool or materials are necessary to install the memory board. A sharp instrument can be used to set the switches. A hand wire-wrap tool is used to strap or unstrap the jumpers.

2.6 Adjustments

No adjustments are necesary.

CHAPTER 3 MAINTENANCE

3.1 Regular inspection

The DTC memory board does not need any special maintenance, other than normally performed with computer systems.
Twice a year the board should be removed from the system. The Q-bus edge connector should be inspected for dust, corrosion or other contaminents and if necessary, cleaned with alcohol (Ethanol 99%) and a soft cloth.

3.2 Hardware testing

The hardware testing is done by installing the memory in the computer system and running the appropriate diagnostic software (see 3.4).

3.3 Software testing

With the memory board no software is delivered. Most DEC operating systems will inform the user how much memory is installed. Some operating systems will use only the memory specified at system generation time. When in doubt, contact your software support centre.

3.4 Required programmes

The memory can be tested by running the diagnostic programme VMSAA0 or higer rev. After successful completion of several passes of this test, it is advisable to test the memory further by running an X11 system test.

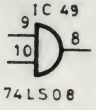
CHAPTER 4 SCHEMATICS

The schematics supplied in this manual are for reference only. Small discrepancies between the schematics and the actual board can occur.

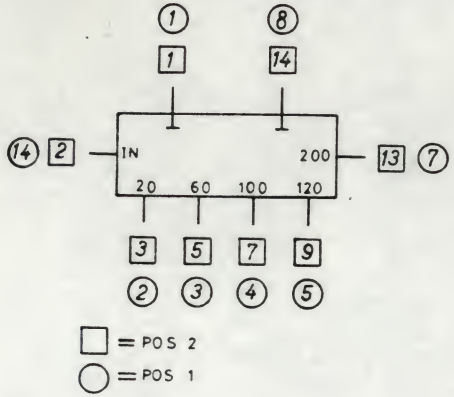
CHAPTER 5 CORRECTIONS

may 83	correction jumper-table 5 and 7	rev a to rev b
jun 83	showing jumpers J10 and J13 corrected for rev c boards	rev b to rev b1
aug 83	hardware modification (ECO #004)	rev b1 to rev c "A" added to p/n

SPARE GATES



IC 39
PIN CONNECTIONS



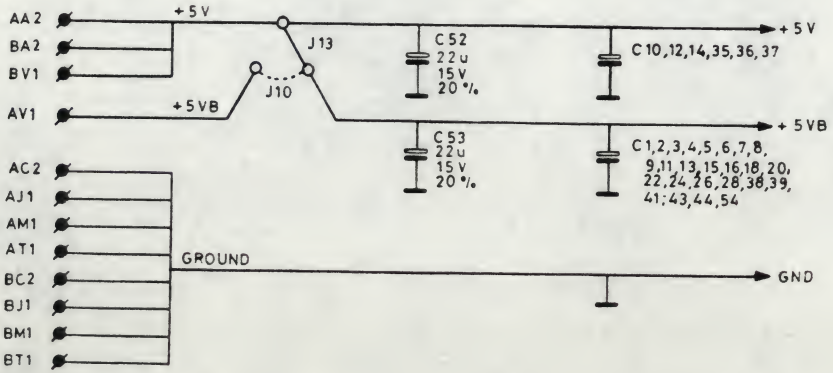
VOLTAGE TABLE

DEVICE TYPE	+12V	-12VB	+5V	+5VB	GND	REFERENCE DESIGNATIONS
DELAY LINE 200NS					1,8of14	IC 39
74S00			14		7	IC 43
74S00				14	7	IC 58
74LS04				14	7	IC 50
74S08				14	7	IC 49
74S30				14	7	IC 64
74S32			14		7	IC 46
74S37				14	7	IC 38 IC 40 IC 41
74S74				14	7	IC 55
74LS74				14	7	IC 56
74S132				14	7	IC 57
74S135			16		8	IC 42
74S175			16		8	IC 48
74LS240				20	10	IC 67
74LS241				20	10	IC 63
74S260				14	7	IC 47
74S283			16		8	IC 44 IC 45
74S373				20	10	IC 51 IC 52 IC 53
74LS393				14	7	IC 54
75452				8	4	IC 66
LM555				8	1	IC 65
2908			20		5,15	IC 59 IC 60 IC 61 IC 62
8641				16	8	IC 68

AM2 BIAKIL
AN2 BIAKOL
AR2 BDMGIL
AS2 BDMGOL

HDA NR.	MEM	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20	J21	J22	TYPE RAM	TE PLAATSEN IC NR'S	MET PARITY	K	L	M
1123	32 KB	N	Y	N	Y	N	Y	N	N	Y	N	Y	N	Y	Y	N	Y	N	Y	N	N	Y	N	2118	1-8,10-17	9,18	N	Y	N
1122	64 KB	Y	Y	N	Y	N	Y	N	N	Y	N	N	N	Y	Y	N	Y	N	N	Y	N	Y	N	4164	1-8,10-17	9,18	Y	Y	N
1121	128 KB	N	Y	N	Y	N	N	Y	N	Y	N	N	N	Y	Y	N	Y	N	N	Y	N	Y	N	4164	1-8,10-17	9,18	Y	Y	N
1120	256 KB	N	Y	N	Y	N	N	Y	N	Y	N	N	N	Y	N	Y	Y	N	N	Y	N	N	Y	4164	1-8,10-17,19-26,28-35	9,18,27,36	Y	Y	Y
1124	32 KB	Y	Y	N	Y	N	Y	N	N	Y	N	N	N	Y	Y	N	Y	N	Y	N	N	Y	N	4164	1-8,10-17	9,18	Y	Y	N
1125	64 KB	N	Y	N	Y	N	Y	N	N	Y	N	N	N	Y	Y	N	Y	N	N	Y	Y	N	N	2118	1-8,10-17,19-26,28-35	9,18,27,36	Y	Y	Y

N = NO
Y = YES



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C55	17,19,21,23,25,27,29,30,31,32
	33,34,40,42,46,47,48,49,5051
S1	
R27	2,3,4,5,6,7
RP2	
W22	
IC68	37

= KONTAKTTONG

PRINTNR.: 19820825-C + ECO 4
19820825-D

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GCMI	27-4-84	HDA 1120 1121 1122 1123 1124 1125	aant.bl.: 4	tek.nr. : 19820826
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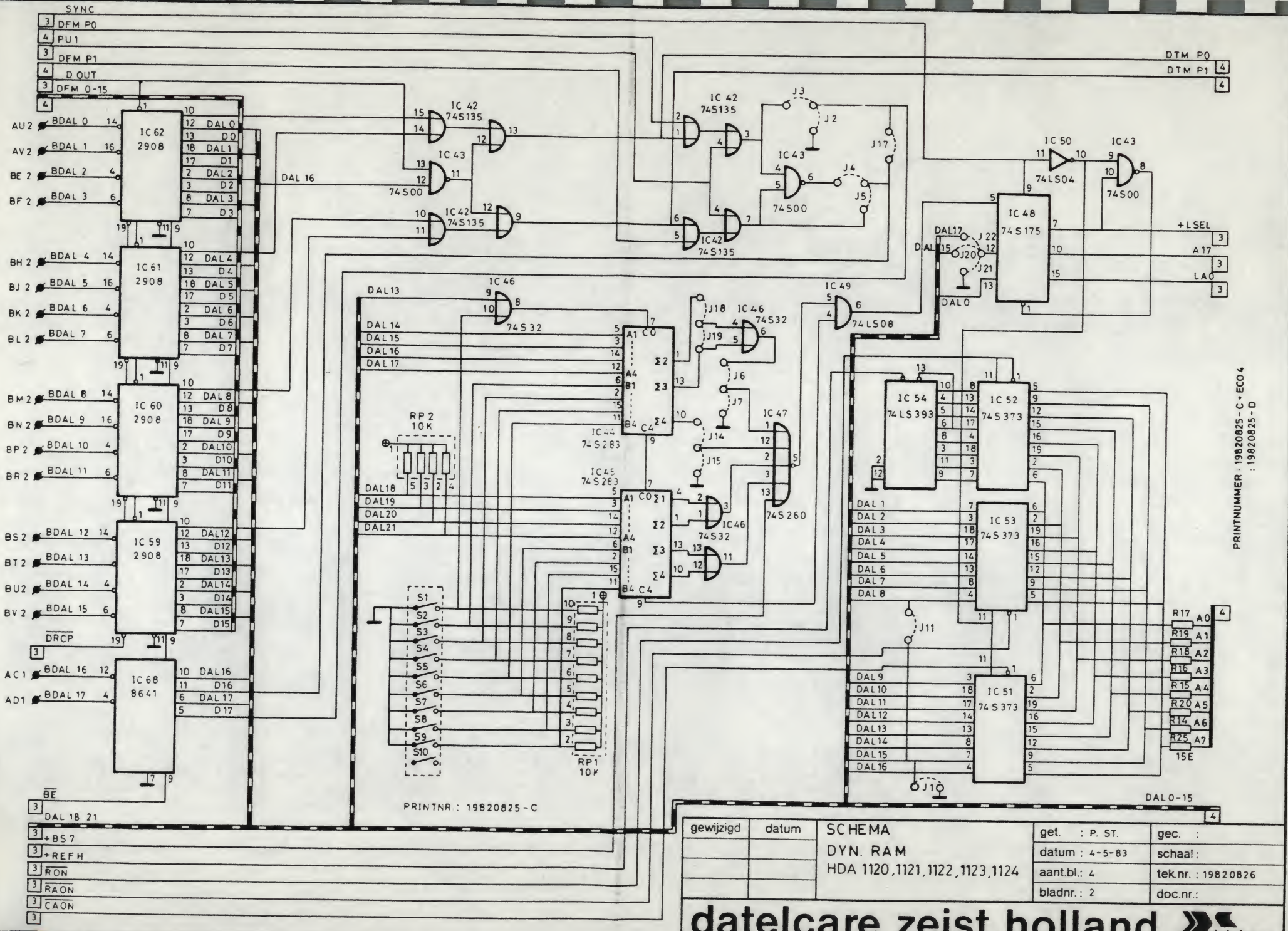

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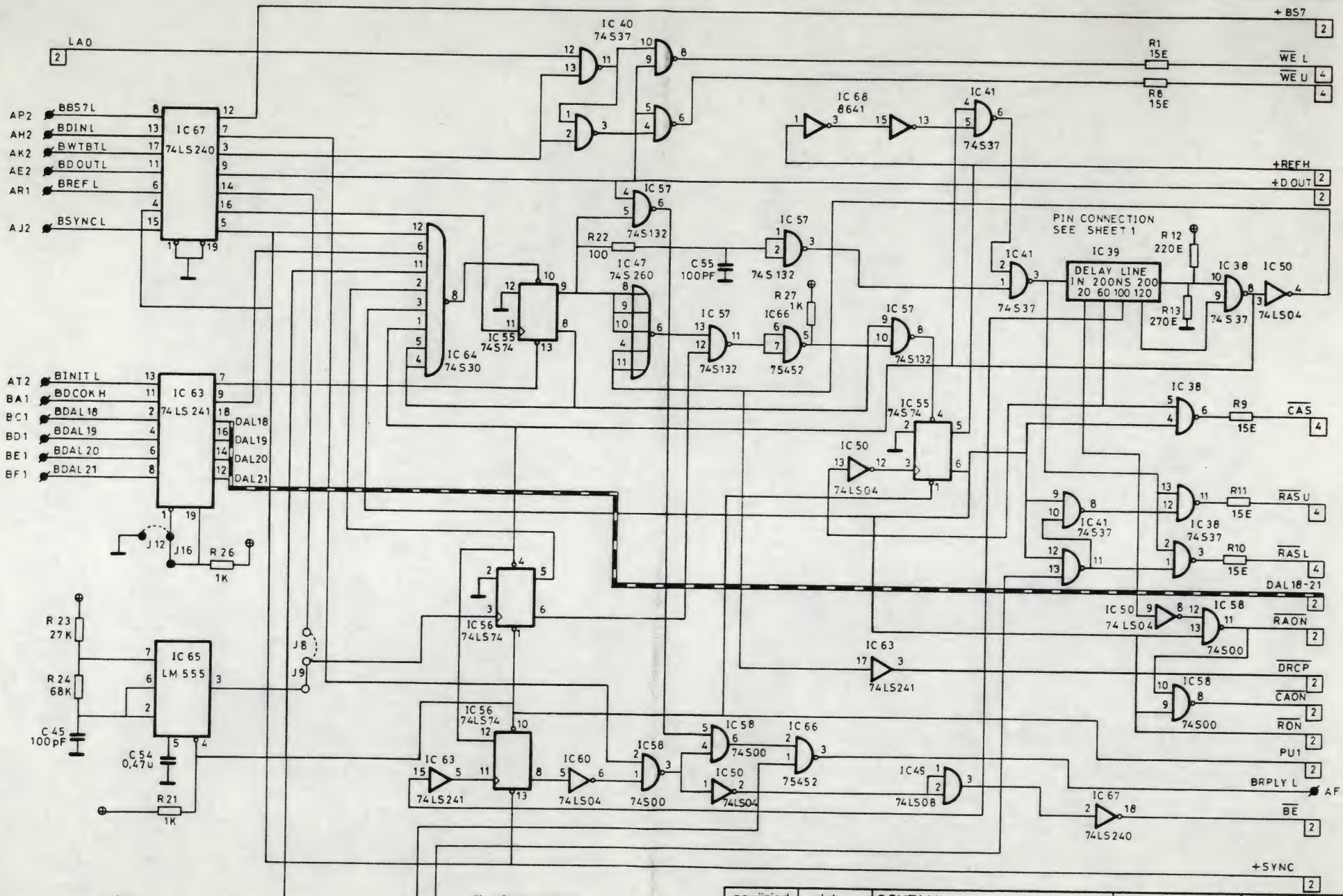

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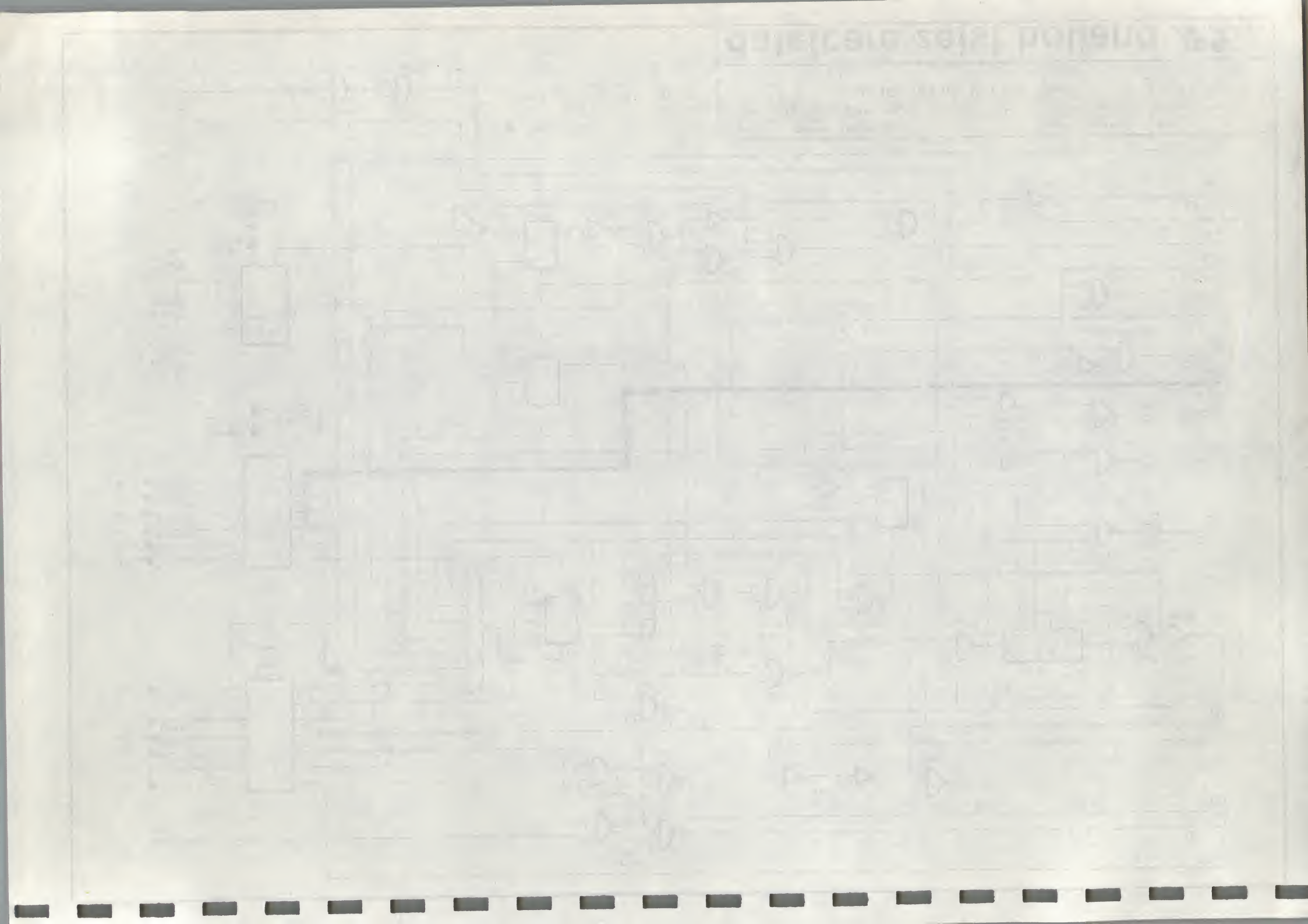
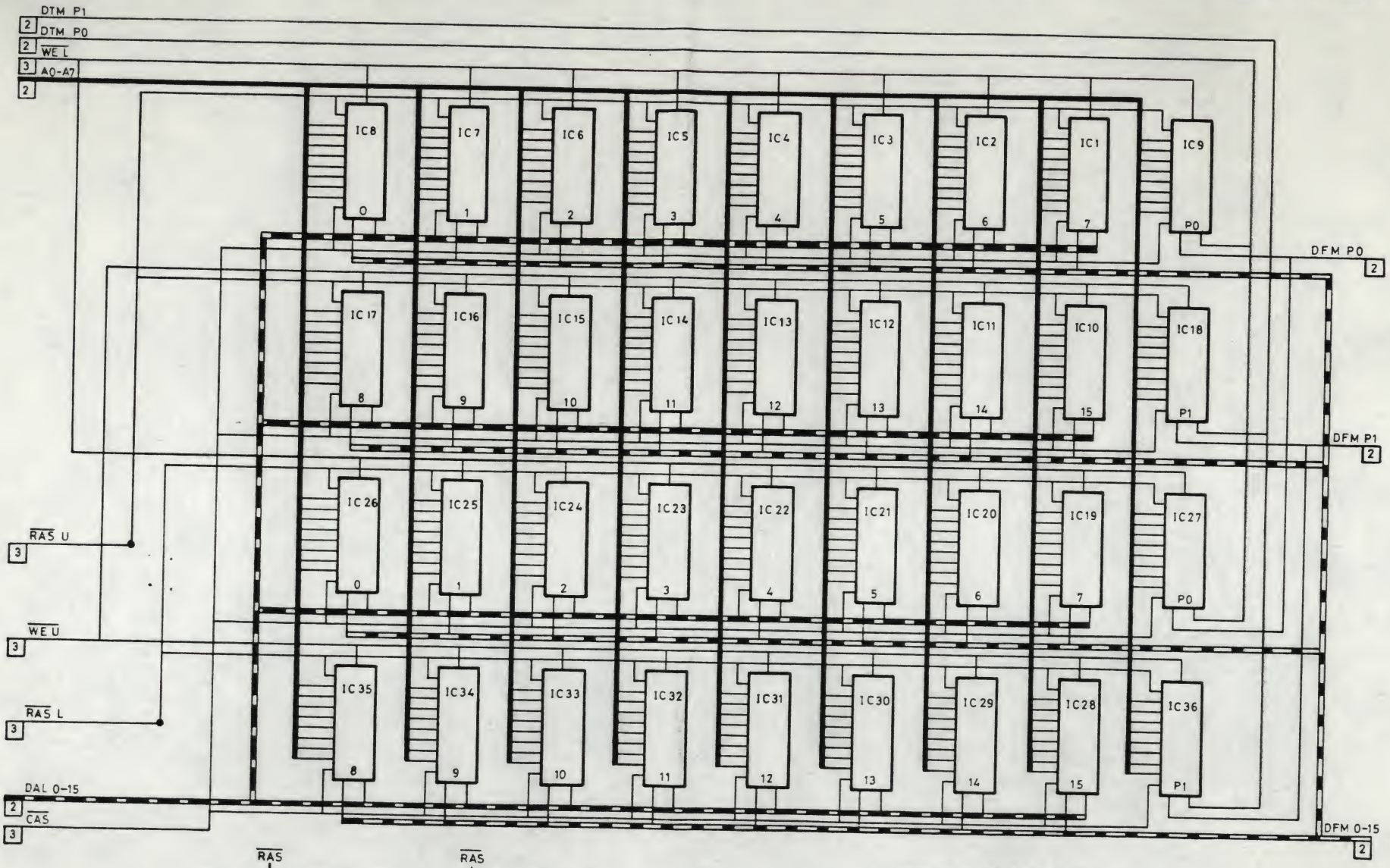
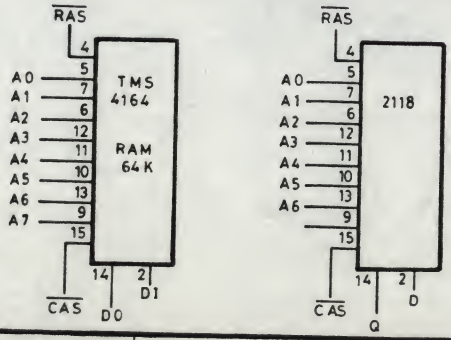




ALLE IC'S PIN 8: +5 VB
PIN 16: GND



PRINTNUMMER: 19820825-C • ECO 4
19820825-D

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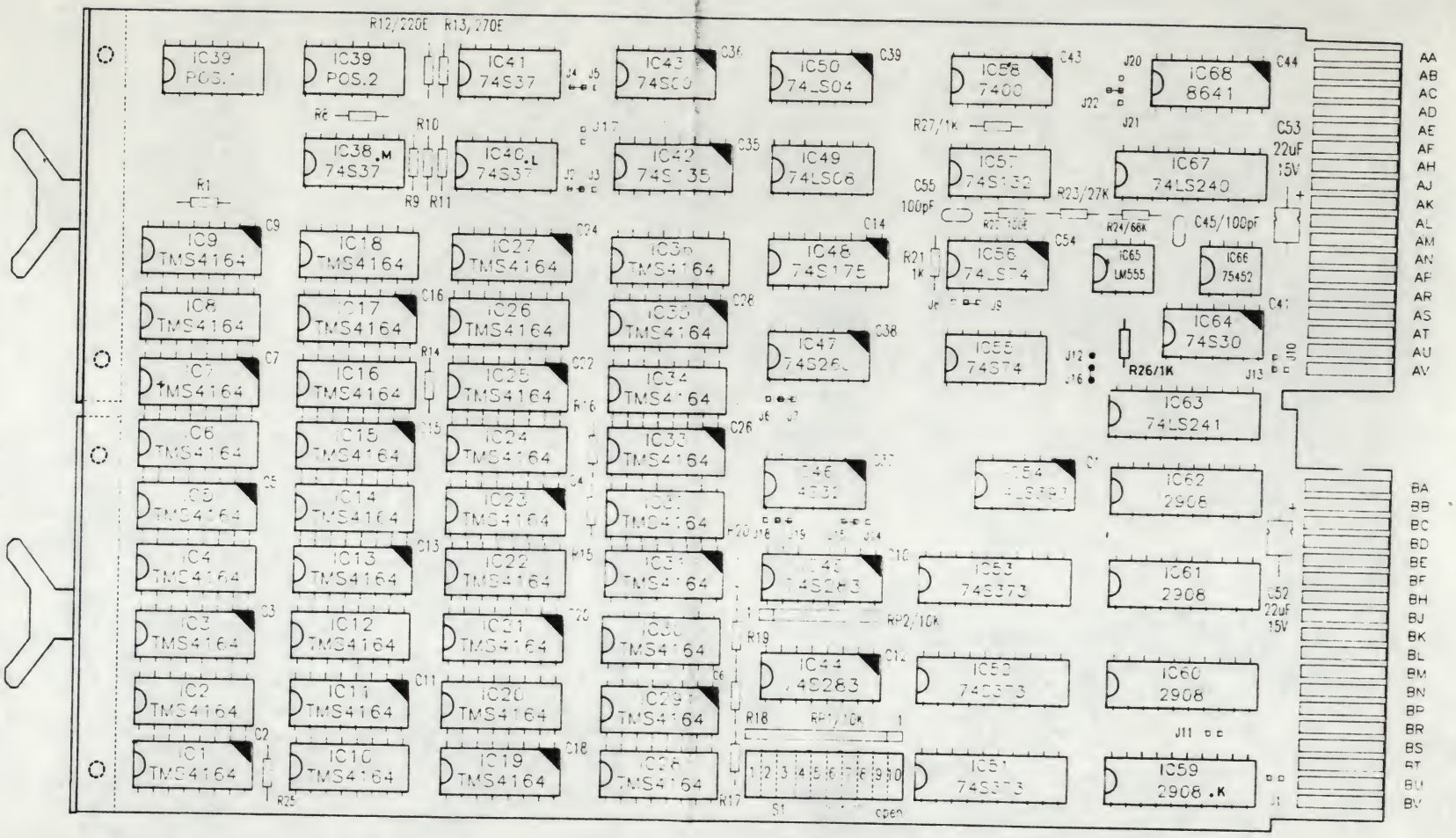

MODIFICEREN VOLGENS ECO 4

ALLE WEERSTANDEN 15E/0,1W TENZIJ ANDERS AANGEGEVEN.

IC56 : EERST C MONTEREN DAARNA R.

GESTIPPELDE ONDERDELEN AAN DE ONDERZIJDE MONTEREN.

◥ = LAYER CONDENSATOR

IC39 : POSITIE 1 - POSITIE 2

EP7071 1-20
5-10
21-29

REVISIENUMMER 01

PRINT NUMMER : 19820825- D

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GCMI	27-4-84	MONTAGEPLAN DYN. RAM 256KB CONCENTRATOR	get. : G.C.M.I.	gec. :
			datum : 25-03-83	school :
			aant.bl. : 1	tek.nr. : 19820827
			bladnr : 1	acc.nr. :

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